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(54) Multistandard decoder for video signals and video signal decoding method

(57) The invention relates to a digital multistandard decoder for composite video signals. The multistandard decoder according to the invention can selectively process NTSC or PAL video signals and there is no need to know the corresponding signal standard beforehand. It comprises a sample rate converter, which converts the sample values of the video signals digitized with a first predetermined clock frequency into video signal sample values of a second virtual sampling frequency, has a phase-locked loop for controlling the sample rate converter, which incorporates a sync detector, in order to determine the line sync pulse and set the virtual sampling frequency to an integer multiple of the line frequency of the video signal, and a burst detector in order to set the virtual sampling frequency synchronously with the phase of the colour subcarrier signal of the video signal, and a decoding - demodulating device for the recovery of the luminance and chrominance signal components from the video signal sample values of the virtual sampling frequency.

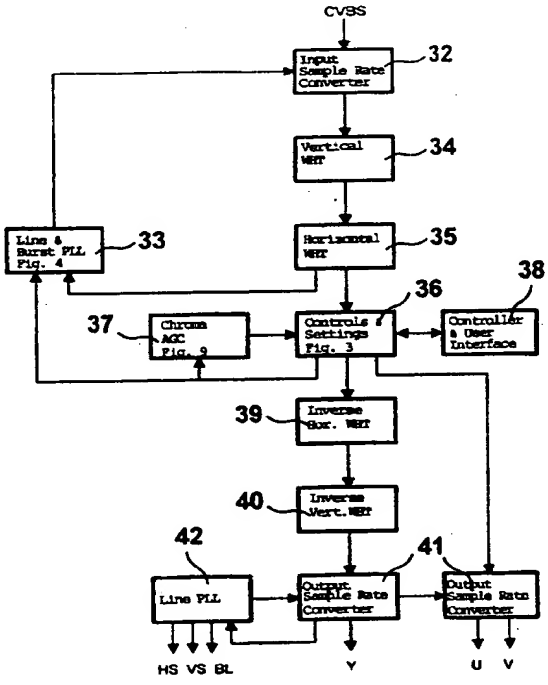

Fig. 2

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In summarizing, Table I gives different sampling frequencies and their advantages/disadvantages for digital video processing:

TABLE I

Sampling Frequency	Advantages	Disadvantages
Burst-locked ($4 \cdot f_{sc}$)	Simple colour decoder. No distortion due to non-linearities.	Complicated line synchronization. A sample rate conversion is necessary for field/frame storages. For multistandard operation multiple crystals are necessary.
	Simple field/frame storage.	
Line-locked ($n \cdot f_H$)	Only one crystal for multistandard operation.	Complicated colour decoder. Sensitive to non-linearities in composite video signal.

The best choice with respect to these factors is dependent on the sought market, the function and intended use of the decoder. A rough survey is given in Table II.

TABLE II

Market	Use	Preferred Sampling
TV set	Replacement of analog circuit.	Burst-locked
TV set	Additional features (field/frame store).	Line-locked
Desk top video (PC)	Fixed video image size in a window.	Burst-locked
Desk top video (PC)	Scalable video image size in a window.	Line-locked

The problem of the invention is to provide a decoder for digital video signals and a composite video signal decoding method, which can process video signals according to different standards on the basis of a random, predetermined clock frequency of a host system, e.g. a PC.

This problem is solved by a digital multistandard decoder having the features of claim 1 and by a method for decoding composite video signals having the features of claim 7.

The invention provides a digital multistandard decoder for composite video signals, comprising a sample rate converter, which converts the sample values of the video signal digitised at a first predetermined clock frequency into video signal sample values of a second virtual sampling frequency, a phase-locked loop for controlling the sample rate converter and which has a sync detector in order to determine the line sync pulse and set the virtual sampling frequency to an integer multiple of the line frequency of the video signal, and which has a burst detector in order to set the virtual sampling frequency synchronously with the phase of the colour subcarrier signal of the video signal, and a decoding - demodulating device for the recovery of the luminance and chrominance signal components from the video signal sample values at the virtual sampling frequency.

Preferably, the decoder according to the invention is so designed that the sync detector comprises a coarse sync detector and a fine sync detector, the coarse sync detector determining the line sync pulse of the video signal, in order to set the virtual sampling frequency to an integer multiple of the line frequency of the video signal (coarse phase control) and the fine sync detector determining an edge of the line sync pulse in order to set the phase of the virtual sampling frequency synchronously with the line frequency (fine phase control), the burst detector determining the phase of the colour subcarrier signal active during the burst pulse, in order to set the phase of the virtual sampling frequency synchronously with the phase of the colour subcarrier frequency (lock-in).

According to an embodiment of the invention the phase-locked loop has a threshold/hysteresis means, which either activates the coarse sync detector or the fine sync detector or the burst detector, said device gives different switching levels for the transition from the coarse phase control to the fine phase control to lock-in than for the transition in the opposite direction.

The given clock frequency can e.g. be the operating clock frequency of a host system for the detector.

It is particularly advantageous if the virtual sampling frequency is four times the colour subcarrier frequency.

The decoder according to the invention preferably has a chroma gain control means, which evaluates the chrominance information of the burst pulse and generates a signal (cokl) which indicates whether the virtual sampling frequency has the desired ratio to the colour subcarrier frequency.

virtual sampling frequency, which corresponds to a given multiple of the line frequency, in which the multistandard decoder can automatically recognize the line frequency of the incoming video signal, so that video signals of different standards can be processed.

The sample rate conversion is a necessary prerequisite for each colour decoder, which does not operate with a fixed predetermined clock frequency generated by a crystal.

According to the invention the sample rate converter is controlled by a hierarchically constructed phase-locked loop, which initially performs a coarse phase control, in that it determines the sync pulse of the video signal and sets the virtual sampling frequency to a clearly defined integer multiple of the line frequency (fh), namely 910·fh for NTSC signals and 1135·fh for PAL signals. Then, by means of a fine phase control, the sampling frequency is set in such a way that a clearly defined phase of the sampling frequency is synchronous to a trigger pulse (of the rising edge of the sync pulse). When the synchronous phase relationship has been established, the colour subcarrier frequency transmitted with the burst pulse is determined and the virtual sampling frequency is produced in phase-locked manner with the phase of the colour subcarrier frequency. In the case of a hierarchic arrangement of the different control planes for the sampling frequency it is very important that simultaneously only one stage is active, so that no chaotic or undefined states can occur.

The invention is described in greater detail hereinafter with respect to a preferred, non-limitative embodiment and with reference to the attached drawings, wherein show:

Fig. 1 A composite EBU colour bar video signal (CVBS) and the corresponding Y, U and V signals, Fig. 1b being a detail enlargement of Fig. 1a.
Fig. 2 A block circuit diagram of a preferred embodiment of the digital multistandard decoder according to the invention.
Fig. 3 A circuit diagram for realizing the control and setting of the decoder of Fig. 2.
Fig. 4 A circuit diagram for realizing the line/burst phase-locked loop of the decoder of Fig. 2.
Fig. 5 A circuit diagram for realizing the coarse synchronous detector of the phase-locked loop of Fig. 4.
Fig. 6 A circuit diagram for realizing the fine synchronous detector of the phase-locked loop of Fig. 4.
Fig. 7 A circuit diagram for realizing the burst phase detector of the phase-locked loop of Fig. 4.
Fig. 8 A curve for explaining the discriminator characteristics of the burst phase detector of Fig. 7.
Fig. 9 A circuit diagram for realizing the automatic gain control for the chrominance signal.
Fig. 10 A circuit diagram for realizing a threshold/hysteresis circuit of the phase-locked loop of Fig. 4.
Fig. 11 A circuit diagram for realizing a phase incrementing circuit of the phase-locked loop of Fig. 4.
Fig. 12 A circuit diagram for realizing a phase integration in the phase-locked loop of Fig. 4.

Fig. 2 shows a block circuit diagram of a preferred embodiment of the digital multistandard decoder according to the invention. The digital multistandard decoder comprises an input sample rate converter (SRC) 32, a line and burst phase-locked loop (PLL) 33, a vertical WHT circuit 34 and a horizontal WHT circuit 35, a control and setting circuit (controls and settings) 36, a chroma automatic gain control circuit 37 (Chroma AGC), a controller and user interface 38, a horizontal IWHT circuit 39 and a vertical IWHT circuit 40, an output sample rate converter (SRC) 41 and a line phase locked loop (PLL) 42.

The composite signal (CVBS) e.g. digitized with the clock frequency of a host system, such as a computer, is inputted into the input sample rate converter 32. The line and burst phase-locked loop 33 controls the input sample rate converter 32, in the manner described hereinafter, so that the input video signal digitized with the predetermined clock frequency is converted into a signal with the sample values of a second virtual sampling frequency, which is four times the colour subcarrier frequency. By choosing the "virtual" sampling frequency as four times the colour subcarrier frequency on the one hand the Shannon-Nyquist theorem ($f_a > 2 \cdot f_{sc}$) is fulfilled and on the other an integer number of sample values per video image signal is obtained, namely 910 sample values per line for a NTSC signal and 1135 sample values per line for a PAL signal, so that it is possible to combine the advantages of a phase-locked architecture, in which the sampling signal is an even multiple of the colour subcarrier frequency, with the advantages of the line-locked architecture, in which the sampling frequency is an integer multiple of the line frequency.

The sample values of the video signal (CVBS) at the virtual sampling frequency are then passed onto the vertical WHT circuit 34, whose output supplies the input signals for the following horizontal WHT circuit 35.

In the vertical and horizontal WHT circuit 34 and 35 the input sample values of the video signal are transformed by means of a 2x4 Walsh - Hadamard transformation (WHT) from the pixel domain into the WHT domain, in which they can be processed by means of the central control and setting circuit 36.

Each individual output coefficient of the Walsh - Hadamard transformation represents a linear combination of all the input sample values (pixels) for said WHT, so that a single WHT output coefficient cannot be associated with a specific input sample value. In fact a set of WHT output coefficients reproduces the two-dimensional spectrum of all the input sample values for a given block of a given size.

a burst phase detector 62. There are also a burst gate circuit 63, a threshold/hysteresis circuit 64 and a phase increment circuit 65, as well as a phase integrator circuit 66 and a divider 67. The connections of the individual circuit components of the line and burst PLL can be gathered from the circuit diagram of Fig. 4, which also shows the chroma automatic gain control circuit 37 (Chroma AGC).

The control of the sample rate converter via the line and burst PLL generally takes place as follows. The virtual sampling frequency is determined in that initially the coarse sync detector 60 separates the sync pulse from the digitized video signal and establishes its time position in order to determine the line frequency. It is then assumed that it is either a NTSC or a PAL signal. For this purpose the user or manufacturer of the decoder can set default values for the sample rate factor, depending on the particular country in which the equipment will be operated, namely at 910 or 1135.

Synchronously with the sync pulse an integral multiple of the line frequency (910·fh or 1135·fh) is produced as a first approximation of the virtual sampling frequency, the coarse sync detector being set with such a wide search window that it always finds a sync pulse.

If the operation of the coarse sync detector 60 is sufficiently stable, there is a switchover to the fine sync detector 61, which determines in a relatively narrow search window on the basis of the approximate position of the sync pulse determined by the coarse sync detector the leading edge of the sync pulse, i.e. the precise time position of the sync pulse and locks the virtual sampling frequency precisely in the edge of the sync pulse.

This prevents side-locking, which could occur in the case of only a phase-locked control of the virtual sampling frequency relative to the phase of the colour subcarrier signal during the burst pulse.

Following stable fine phase control the phase of the colour subcarrier frequency can be determined by the burst phase detector 62 and the sampling frequency can be set synchronously to this phase, the burst pulse representing a time window during which the colour subcarrier reference signal is transmitted. The thus determined, virtual sampling frequency and phase are outputted as a control signal to the sampling rate converter 32.

The individual circuit components of the line and burst PLL of Fig. 4 and their operation are described hereinafter relative to Figs. 5 to 12.

Fig. 5 shows a circuit diagram of the coarse sync detector, which determines the line sync pulse of the video signal. Upstream of the coarse sync detector are five series-connected delay stages 70 to 74, through which passes the $WHT_{0,0}$ coefficient and which is then further processed in the coarse sync detector. The circuit of Fig. 5 also comprises two comparators 75, 76, an AND gate 78, a comparator 79 and a series connection of an adder 80, a binary divider 81 and a delay element 82, which are interconnected as shown in Fig. 5.

The WHT coefficient $WHT_{0,0}$ outputted by the horizontal WHT circuit 35 corresponds to a horizontally low-pass-filtered version of the CVBS input signal of the digital decoder. At the end of setting and synchronization of the virtual sampling frequency the WHT coefficient $WHT_{0,0}$ corresponds to a horizontally and vertically low-pass-filtered version of the CVBS signal. In each case $WHT_{0,0}$ is used for suppressing the high frequency colour subcarrier, which would otherwise possibly disturb the detection of the line sync pulse. The limited bandwidth of the WHT coefficient $WHT_{0,0}$, which is determined by the order of the upstream Walsh - Hadamard transformation, also determines a nominal edge slope of the line sync pulse and prevents possible peaks in the input signal.

The coefficient $WHT_{0,0}$ forms the input signal for the line sync pulse processing. A leading, falling sync edge is determined if the comparators 75 and 76 indicate that at least two successive values of $WHT_{0,0}$ are higher or equal to a sync switching level (< 2·bl), a following value of $WHT_{0,0}$ has a random value and at least two further following values of $WHT_{0,0}$ are smaller than the sync switching level (< 2·bl). The sync switching level is defined as the value between the black level and the peak value of the sync pulse, as shown in Fig. 1b.

In order to reduce the susceptibility to possible signal peaks and to fade out equalizing pulses, the coarse sync detector of Fig. 5 is only active if the phase integrator exceeds a value of "640". In this case the comparator 79 emits a "1" signal. If the above conditions for a falling sync edge are fulfilled, then a sync trigger signal (csd%) is outputted. In addition, the difference (csd0) of the phase integrator value with respect to the nominal number of sample values per line (910 or 1135), as shown in Fig. 5, is stored and transferred, in order to indicate the instantaneous phase relationship between the line sync pulse and the phase integrator for controlling the sample rate converter. The loop gain is set by means of the binary divider 31 by a 12 bit offset to 1/4096.

If the coarse sync detector of Fig. 5 has determined a line sync pulse and outputted a sync trigger signal, the fine sync detector of Fig. 6 is activated in order to synchronize the virtual sampling frequency precisely with the leading edge of the sync pulse. It forms a PI controller for controlling the virtual sampling frequency synchronously to the line frequency of the video signal.

The fine sync detector shown in Fig. 6 comprises five adders 83 to 87, two delay elements 88, 89 and two binary dividers 90, 91, shown in interconnected form in Fig. 6.

From the sum of the $WHT_{0,0}$ values delayed by three and four clock pulses is subtracted the sum of the undelayed $WHT_{0,0}$ value and its counterpart delayed by five clock pulses, as shown in Fig. 6. As the phase increments are accumulated before being inputted into the phase integrator, the proportional value must be produced by means of a differentiation 86, 88, whereas the integral value is directly accessible.

The phase increment or incrementing circuit is shown in Fig. 11 and comprises a multiplexer device 108 and an integrator 109 constituted by an adder and a delay stage, which is switched on by the burst gate signal. Corresponding to the thresholds defined by the threshold and hysteresis circuit the multiplexer device 108 selects one of the three input signals from the coarse sync detector 60, the fine sync detector 61 or the burst phase detector 62. The phase increment, in accordance with the coarse, fine or burst phase different signal, is updated once during each horizontal line, controlled by the burst gate signal, and outputted to the phase integrator.

The phase integrator circuit shown in Fig. 12 comprises an adder 110 and a delay stage 111, which can be interconnected in the shown manner. The phase integrator serves as the digitally controlled oscillator, which produces the virtual sampling frequency of $4 \cdot f_{sc}$, i.e. $910 \cdot fh$ or $1135 \cdot fh$, for the sample rate converter. The phase integrator is timed by the burst gate pulse and accumulates the phase increments determined in the preceding stage. If the phase-locked loop is already locked in, the phase integrator accumulates increments up to an integer value of 910 or 1135. Additionally the intermediate pixel resolution of the sample rate converter 32 (Fig. 2), which according to a preferred embodiment of the invention is 1/32 (5 bits), a non-integer output of the phase integrator. The phase integrator circuit requires in the represented embodiment an overall resolution (precision) of 29 bits, 12 bits being required for the integer and 17 for the non-integer integrator output values.

As shown in Fig. 12 the sync trigger signal outputted by the coarse sync detector resets the integer bits of the accumulator, but the non-integer bits remain unaffected.

The carry of the phase integrator, i.e. the carry from the non-integer to the integer components, determines a time at which a given sample value for a sampling frequency of $4 \cdot f_{sc}$ is to be calculated by the input sample rate converter. The non-integer component of the output signal of the phase integrator specifies the intermediate pixel distance of the "virtual" sample value from an actual sample value as fractions of the host clock frequency.

However, the sample rate converter requires a control input value, relative to the output sampling rate ($4 \cdot f_{sc}$). As the phase increment indicates the relationship of the host clock frequency to $4 \cdot f_{sc}$, it is necessary to divide the non-integer component of the output value of the phase integrator by the value of the phase increment. This division is performed by the divider 67. The accuracy of this division must enable the sample rate converter to produce intermediate pixel increments of 1/32 (5 bits). In order to form an output signal with a precision of 5 bits, the input precision of the divider must be 7 bits for the numerator and 8 bits for the denominator.

The input sample rate converter 32 can be in accordance with the prior art. A particularly simple and advantageous sample rate converter suitable for digital multistandard video decoders is described in the parallel application of the same applicant and having the same application date entitled "Sample rate converter and sample rate conversion process" to which is incorporated herein by reference. Such a sample rate converter performs an equally weighted interpolation between each of two neighbouring sample values and subjects to an amplitude correction the interpolation result obtained. Then a further equally weighted interpolation of the corrected, first interpolation result is performed with its neighbouring values and these can be neighbouring sample values or neighbouring interpolation results and the interpolation result obtained then again is subject to an amplitude correction. The equally weighted interpolation is then repeated until the desired resolution necessary for the virtual sampling frequency is reached, e.g. 1/32 of the host clock frequency. The control signal for the sample rate converter outputted by the phase-locked loop then determines the direction and magnitude of an offset for in each case one virtual sample value relative to an actual sample value.

At the output of the digital multistandard decoder according to the invention can once again be provided a sample rate converter controlled by a line and burst PLL, if the decoded video signal is to be further processed at a clock frequency other than $4 \cdot f_{sc}$.

However, it is also possible to provide a simplified output sample rate converter 41 controlled by a line phase-locked loop 42 (Fig. 2). In the line PLL corresponding parts of the described line and burst PLL, namely the coarse and fine sync detectors are repeated, said parts being copied for the line PLL, but cannot be directly reused, because they must continuously monitor the burst PLL. For the output sample rate converter it is possible to use a simple linear interpolation between adjacent pixels, because only baseband signals Y, U and V and not composite video signals (CVBS) have to be processed, which with the colour carrier frequency contain information with a high spectral component, which occurs after demodulation as a d.c. voltage. The requirements made concerning the linearity of the frequency-dependent gain function of the sample rate converter are therefore much less.

The features of the invention disclosed in the description, drawings and claims can be significant, either individually or in the form of random combinations, for the realization of the different embodiments of the invention.

Claims

1. Digital multistandard decoder for composite video signals, comprising a sample rate converter (32), which converts the sample values of the video signal digitized at a first predetermined clock frequency into video signal sample values at a second virtual sampling frequency, a phase-locked loop (33) for controlling the sample rate converter and which has a sync detector in order to determine the line sync pulse and set the virtual sampling frequency to an integer multiple of the line frequency of the video signal, and which has a burst detector in order to set the virtual

14. Method according to any one of the claims 7 to 13, characterized in that the virtual sampling frequency is set as 910 or 1135 times the line frequency of the video signal.

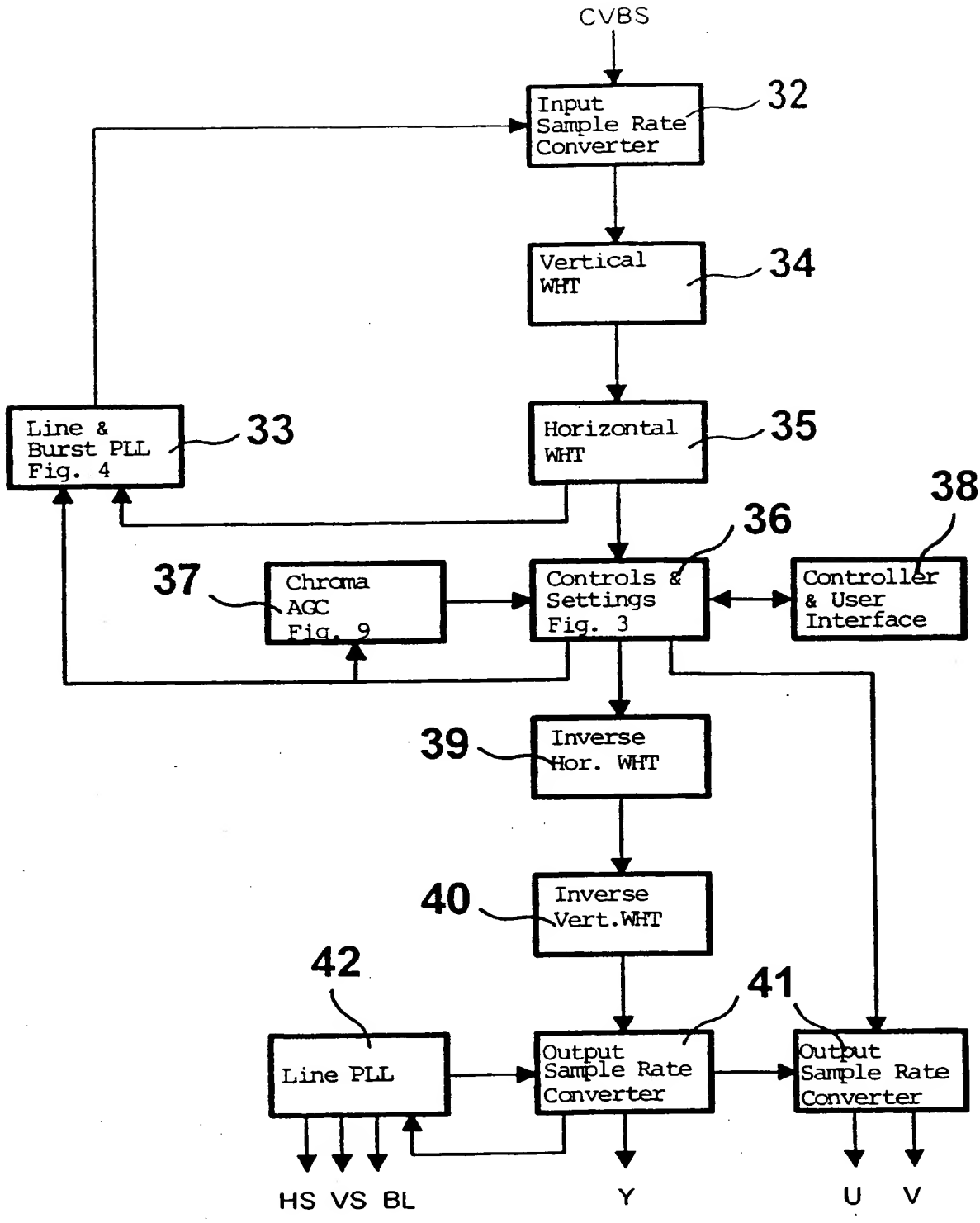
CVBS
Input Sample Rate Converter
32
Vertical WHT
34
Horizontal WHT
35
Line & Burst PLL Fig. 4
33
38
36
37
Chroma AGC Fig. 9
Controls & Settings Fig. 3
Controller & User Interface
39
Inverse Hor. WHT
40
Inverse Vert.WHT
42
41
Line PLL
Output Sample Rate Converter
Output Sample Rate Converter
HS VS BL
Y
U V

Fig. 2

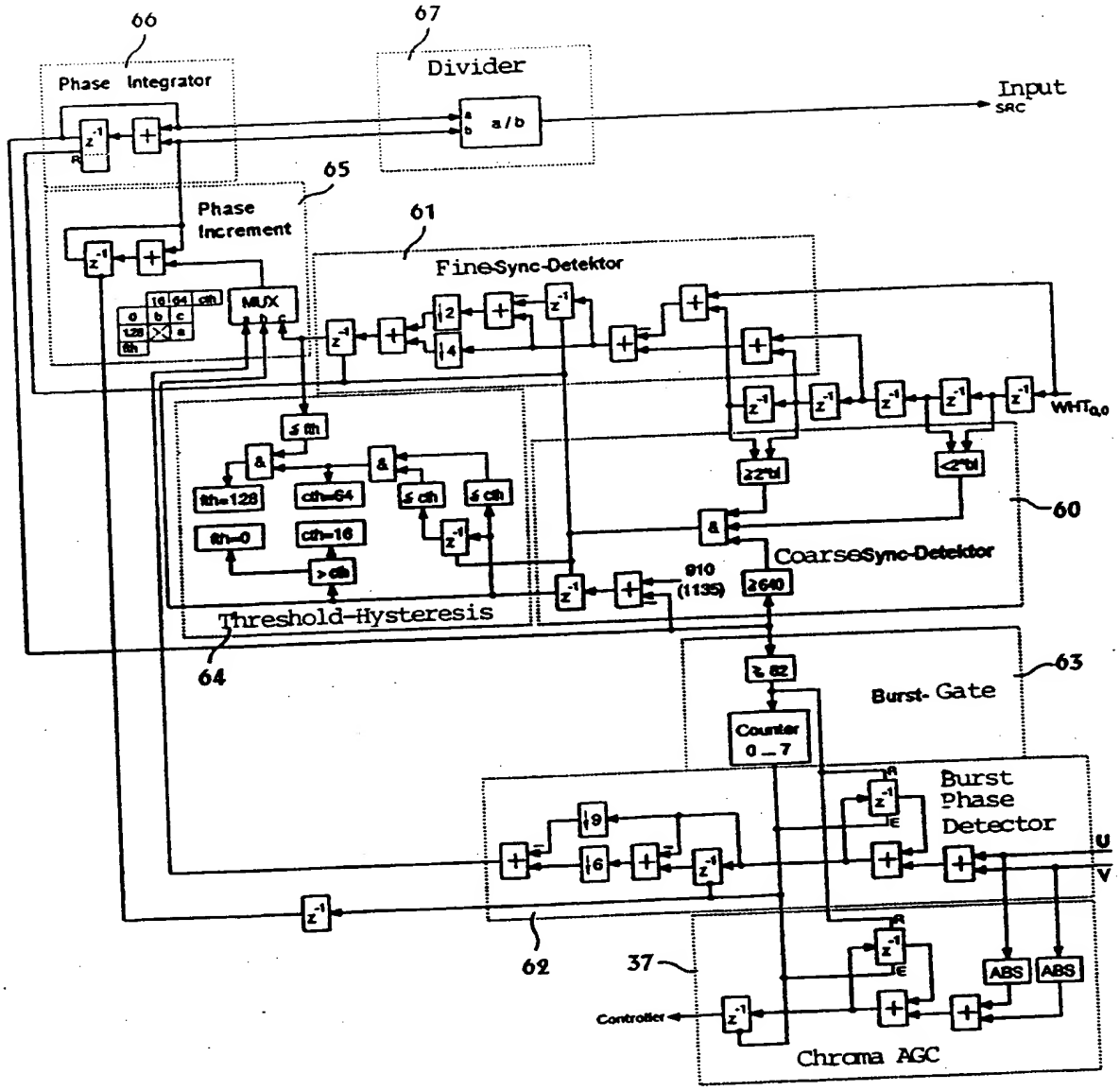
66
Phase Integrator
67
Divider
a/b
Input
SRC
65
Phase Increment
61
FineSync-Detektor
MUX
WHT0,0
60
CoarseSync-Detektor
910
(1135)
2640
Threshold-Hysteresis
64
63
Burst-Gate
Counter
0 – 7
Burst
Phase
Detector
U
V
62
37
ABS
ABS
Controller
Chroma AGC

Fig. 4

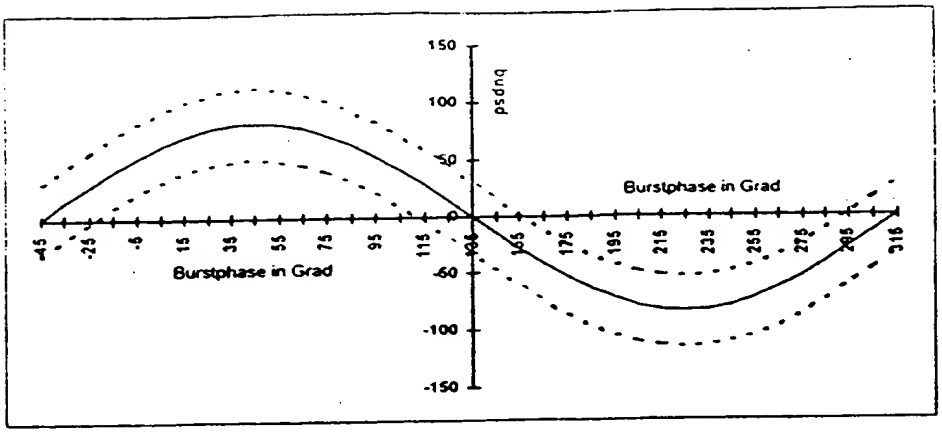

Fig. 8

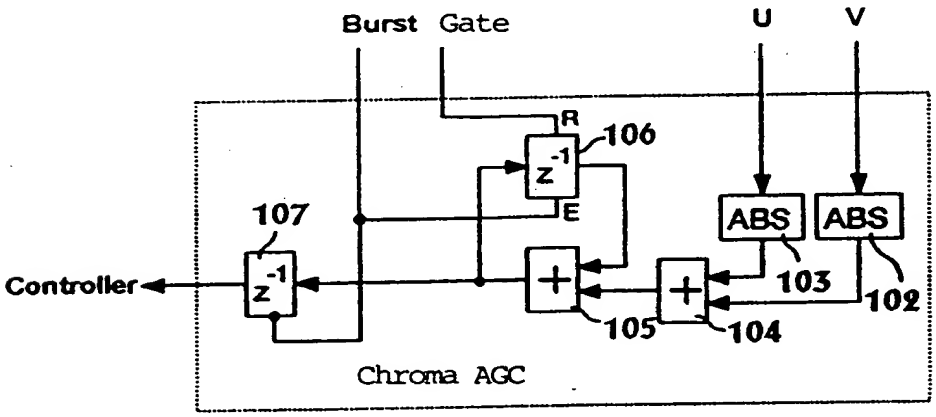

Fig. 9

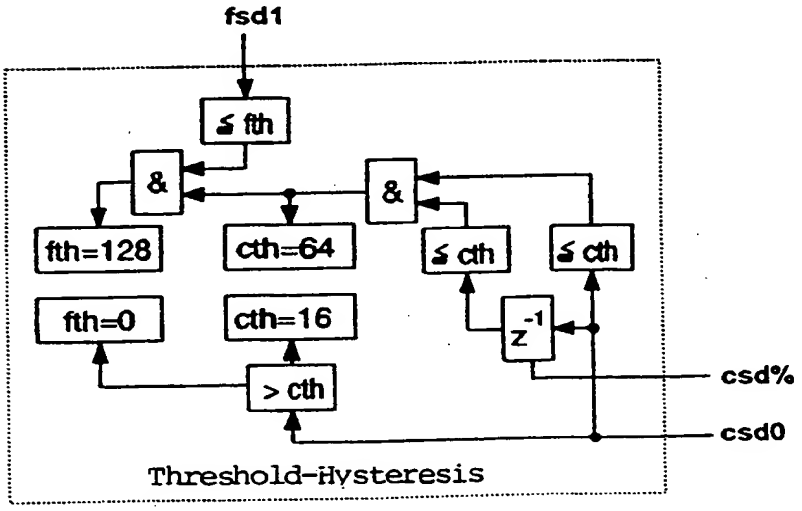

Fig. 10

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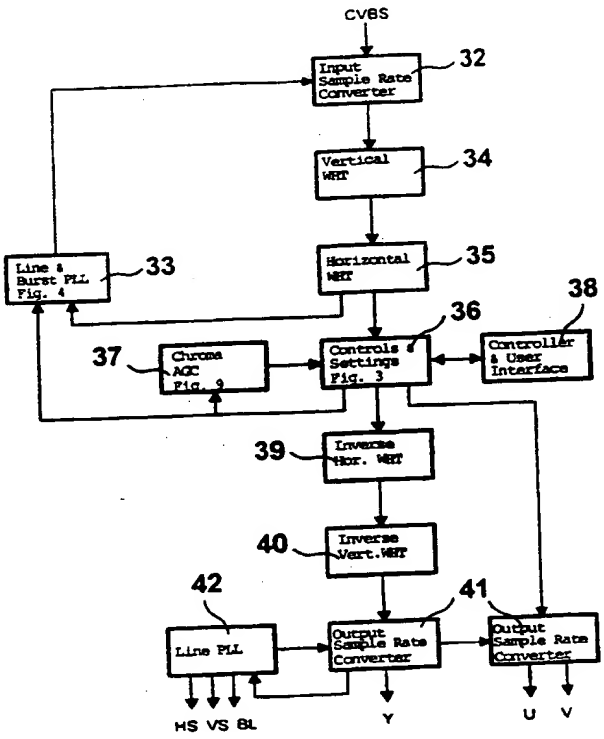

Fig. 2

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